VIDEO OUTPUT - 1400

The video output board consists of three DC-coupled amplifiers that accept the Red, Blue, and Green signals and then drive the cathodes of their respective cathode-ray tubes with them. The board also blanks the output signals during horizontal and vertical retrace.

Since each amplifier is identical, only one channel needs to be discussed. The circuit can best be analyzed as an operational amplifier used in the inverting configuration. The input signal is applied across R3, R4, and C1, creating a current into the virtual ground at TP 2. Since Q1 draws essentially no current, this current is equal to the current from the virtual ground through C6 and R10. The voltage gain of approximately 35 is due to the fact that the input current is matched by a current made to flow across R10's higher impedance, 33K. C6 is used to swamp out any stray capacitance associated with the large one watt R10. Since C6 also rolls off the gain of the amplifier at high frequencies, C1 is used to provide a high end boost for the input signal.

Inside the "operational amplifier", Q1 and Q2 act as a differential pair, the output of which is developed across R6. This voltage is fed to Q4, which drives the cathode and the feedback network. Q3 is a current source collector load for Q4, and it is this configuration that supplies the high open-loop gain necessary for an operational amplifier. However, note that while Q4 can pull down the output quite strongly, the maximum pull-up is limited by the current available from the current source (equal to .6V/68Ω, or 10 ma). To provide a better slew rate at high frequencies, C2 couples some of the signal on the base of Q4 to the base of Q3, thus modulating the current source.

The 8V reference voltage common to the video output board and the RGB processor board serves two important functions. First, note that, by itself on this board, the reference voltage is approximately 10V. When the video output and the RGB processor are connected, the zener diode on the RGB processor draws current until the voltage on both boards is nominally 8V. Thus if the RGB processor board is removed while the set is in operation, the voltage on the base of Q2 immediately rises several volts and the cathode-ray tubes are driven to black. Second, observe in Figure 1400-1 that the transistor on the RGB processor board is biased by the 8V reference voltage. Since Q1 has the same DC voltage on its base as does Q2 (by differential action), the drive control on the RGB processor board has the same DC voltage on each side. Thus as the drive control is rotated no DC current flows into the video output board, and an AC change is effected while the DC level is held constant (nominally 150V at TP 4).

Finally, blanking is accomplished by Q13, which saturates and draws a certain amount of current (8V/4k7 = 1.7 ma) from the node at TP 2. This extra current must come from TP 4 through R10 - thus the output rises approximately 50V (33k x 1.7 ma) and the tubes are blanked off. Q13 is turned on by a 30V line-rate pulse at pin 13 and also by a 30V field-rate pulse at pin 15. C21 and R46 serve to remove tilt from the vertical pulse base line, while R45 and C20 low-pass filter pincushion information.

The video output board is protected against arcs inside the tubes by 100Ω resistors in series with the cathodes and by .75pf spark gap capacitors in parallel with the cathodes.

CROSS-HATCH GENERATOR - 1500

The cross-hatch generator board generates a video cross-hatch pattern signal for focusing and static convergence adjustments. The circuit derives its timing information from the deflection circuitry, and, although the board will continue to function, if a pattern is to be projected it is necessary that the sweeps be synchronized to a stable time base, i.e., an off-the-air program or an external signal.

The horizontal lines generator consists of a four-bit binary counter which, in conjunction with D4-7, R9, R21, and Q1, produces an output pulse every 16 lines. The 30V horizontal retrace pulses at pin 5 are divided down by R1 and R3 and clamped to +15V by D1. Since IC-1 is floated above ground by zener diode D3, these pulses represent transitions between logic state 0 (+10V) and logic state 1 (+15V). Applied to pin 1, the pulses toggle the flip-flops of IC-1 with negative-going transitions. The resultant pulses at pins 9 (÷1), 11 (÷4), and 12 (÷8) are OR-gated to Q1's base, while pin 8 (÷2) is coupled to the emitter. This logic leads Q1 to turn on once every 16 lines, and as a result a pulse appears across R21. Synchronization with the vertical sweep is accomplished by first differentiating (C1-R5) and filtering (R6-C2) the vertical retrace pulse and then by applying it to pin 3. This pulse, together with the horizontal pulses on pin 2, triggers a NAND gate in IC-1 that resets the counter every field.

The vertical lines generator is a large mark-to-space ratio astable multivibrator with a synchronizing input. The "on" and "off" time constants are determined by C6-R15 and C6-R17/R18 respectively; thus R18 sets the vertical line spacing. Synchronization is achieved by coupling the 30V horizontal retrace pulse to Q4's emitter, where it insures that Q4 is held off. When Q4 turns on and charges C6 through R15, the voltage drop across R16 saturates Q5. The resultant current through R19 creates an output voltage pulse across R21.

D8, C7, and R22 form a clamp which assures uniformity of amplitude between horizontal and vertical line pulses (approximately 1.5V p-p), while Q2 provides blanking during both horizontal and vertical retrace times.

VERTICAL OSCILLATOR AND AMPLIFIER - 1600

Vertical scan current is generated and maintained in precise synchronization with incoming video by the vertical oscillator and amplifier board. Transistors Q1, Q2, and Q3 serve as vertical sync separator, generating a vertical trigger pulse from composite sync. Q4, Q5, and Q6 form the vertical oscillator, and Q7, Q8, and the two external transistors comprise the vertical amplifier. The sync waveform is coupled through C1 into the junction of D1 and R1. D1 conducts, preventing the sync from going more positive than +30V. During a sync pulse, when the sync waveform is high, R1 has approximately 0V across it, and Q1 is turned off, allowing R2 to start charging C2. When the sync pulse is over, C1 couples the 30-volt negative step to R1, which puts a voltage across R1 of about 25V, turning on Q1. Q1 then discharges C2 through R3. The time constants of the circuit are arranged such that during a horizontal sync pulse (or equalizing pulse) the voltage on C2 never approaches the voltage determined by R5, R6, and Q2's V_{be}, so Q2 does not conduct. During the vertical sync pulse, Q1 is off for a long enough time to allow C2 to charge to about 1-½ volts, turning on Q2. With Q2 on, C4 is rapidly charged to about 26 volts, and the vertical pulse is generated. Q3 is a phase inverter which couples a negative pulse into the second base of unijunction transistor Q4.

At the heart of the vertical oscillator is unijunction transistor Q4. A UJT consists of an ohmic region (from $base_1$ to $base_2$) and a PN junction (from the emitter to the ohmic region). See Figure 1400-1. The equivalent "off" state circuit is given by Figure 1400-2. It can be seen that as long as the emitter voltage is less than the intrinsic standoff ratio, η, times the voltage between b_1 and b_2, then the PN (diode) junction is non-conducting. Should the emitter voltage increase beyond this point (see Figure 1400-3), then the diode conducts, injecting minority carriers into the base region, which causes it to become highly conductive. The device is then in its negative resistance region, and it will remain there as long as it is supplied with the necessary voltage and current required to keep it in conduction.

Transistor Q5 is configured as a current source with the amount of current determined by the vertical hold control. Q5 charges C5 until the voltage on the emitter of Q4 is equal to the standoff ratio times the voltage on Q4's $base_2$, at which time Q4 conducts and quickly discharges C5. The cycle of charging and discharging starts again because the voltage and current through Q4 which was supplied by C5 is no longer enough to sustain conduction in the UJT. Q4 can be turned on prematurely by means of a negative trigger pulse applied to the second base, which will lower the value of emitter voltage required to fire Q4. Q6 is an emitter follower which takes the high impedance ramp signal and buffers it, feedling it to DC blocking capacitor C7 and out to the height control.

The vertical amplifier consists of current-summing amplifier Q8, current source Q7, and the two external power transistors. Signal flow is from the transistor emitter resistors and the fuses to the series connected yokes and the pincushion board through the 1000 μFd. capacitor, returning to pin 7 and R25 to ground. Current flowing through the yokes also flows through R25, developing a voltage across it which is proportional to the yoke current. This voltage is then coupled back by R24 to the base of Q8. Q8 is a single-stage inverting amplifier whose collector is fed from current-source Q7 and is also connected to the bases of the external power transistors. Q8's gain is determined by the ratio of the input signal source impedance (R21 and the height control) to R24. R23 serves to DC bias the amplifier, and because the 1000 μFd capacitor charges somewhat, the AC component of the ramp on Pin 6 is not exactly proportional to yoke current, thereby introducing a non-linearity into the amplifier which is corrected for by R17, R16, and C6. These components put a small ramp on the base of Q5 which modulates the amount of charging current available for C5, adding a second harmonic component to the oscillator output which is out of phase with the original non-linearity. Note that *current* sensing and feedback is used. It is necessary to control yoke current instead of yoke voltage because of the large inductive component of the vertical deflection yoke impedance.

The external diode serves to clamp the vertical flyback pulse to +40V, thereby reducing the strain on the NPN power transistor. The bypass capacitor (.068 MFd) has no effect on the vertical ramp, but effectively bypasses horizontal-rate vertical pincushion correction signals.

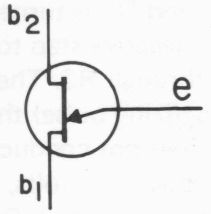


Figure 1

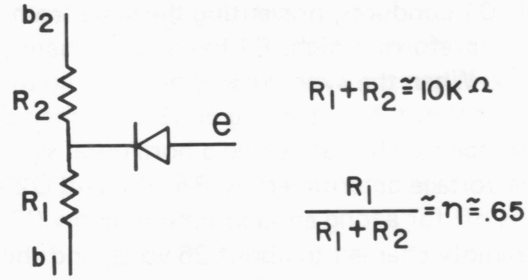


Figure 2

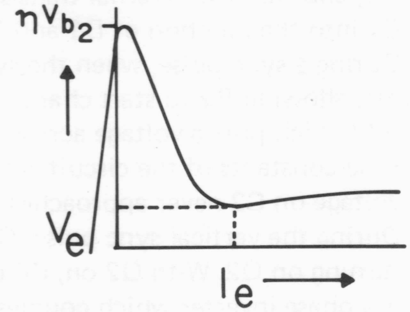


Figure 3

HORIZONTAL OSCILLATOR - 1700

The horizontal oscillator board generates repetitive pulses which are used to trigger the horizontal output assembly (A1800) and compares the resultant horizontal sweep to incoming line-rate sync pulses, maintaining phase-lock (and thus synchronization) between them. The circuit is a phase locked loop consisting of phase detector Q1, D1, D2, low-pass filter C6, R11, C7, oscillator Q2, and feedback element horizontal output assembly, connected to pin 3. Also included is an over-voltage protection circuit which senses anode voltage and in the event of excessive voltage shuts off the horizontal oscillator (and thus the anode voltage).

A thermally compensated voltage across R16 and TR1 is applied to the horizontal hold limit potentiometer. The setting of this control and the value of R14 determine the amount of DC current injected into the base of oscillator transistor Q2. This current charges C8 until enough voltage is applied to Q2's base to turn Q2 on, at which time, because of positive feedback from T1, Q2 "snaps" on, producing a large positive pulse across T1's output winding. After T1 saturates (about 4 μsec after turn-on) the base winding develops a sharp negative voltage spike, which quickly turns Q2 off and discharges C8. C5, L1, L2 and damping resistors R9 and R10 form a ringing circuit which acts to stabilize the turn-on of Q2 by adding in a large positive-slope voltage. (See Figure 1700-1). The output pulse on T1's tertiary winding goes to D5, R48, and C10, which serve to shape the pulse such that it is suitable for triggering the commutating SCR.

The phase comparator consists of transistor Q1 and diodes D1 and D2. The approximately 500V horizontal retrace pulse applied to pin 3 is integrated by C15 to form a ramp. This ramp is amplified and inverted by Q3 and then biased slightly below ground by R35 and R36. The 8V p-p positive-going ramp has a negative-going retrace which is coupled by Q4 into the sample and hold circuit (Q1, D1, and D2). Diodes D1 and D2 are normally non-conducting, but during a sync pulse, Q1's emitter goes positive and its collector goes negative. The step transition is coupled by C2 and C3 to D1 and D2, causing them to conduct. This clamps the ramp to R6 and R7 which charges C6. At the end of the sync pulse, D1 and D2 open up, but C6 remains charged. Zero correction voltage is produced only when the zero-crossing of the ramp generated by the horizontal retrace pulse is coincident with the end of the horizontal sync pulse. Any voltage other than zero adds to or subtracts from the current injected into Q2 by the horizontal hold control(s) thus correcting its frequency of oscillation. D3 and D4 limit the maximum correction voltage to + or - 0.6 volts. The horizontal AFC loop time constants are set by C6, C7, and R11. These values are chosen to give a realistic compromise between good noise immunity and wide pull-in range.

The high voltage shut-down circuit consists of transistor Q6 and silicon-controlled rectifier SCR1. The high voltage cage and cover assembly develops a voltage proportional to anode voltage (at the multiplier terminal labeled "focus") which is turned into a current and fed into pin 12. The sensing current flows through R19, R20, R21 and R22, generating a voltage which is proportional to that current. D6, R19, and R20 act as an isolating clamp which during arc conditions, limits voltage transients which would otherwise unnecessarily trigger the shutdown circuit. R21 controls the amount of voltage fed to the emitter follower, Q6. Zener diode D7 sets a threshold voltage above which it will conduct and fire the SCR. SCR1 discharges C13 and shorts out the horizontal oscillator B+ voltage. (Note that the +30V for Q2 is derived from the +160 volt supply. This is done to insure quick starting of the oscillator.) With no trigger pulses high voltage generation ceases, thereby removing the overload condition; however SCR1 remains in conduction until forward current is removed from the SCR. This may be achieved by turning off the set and waiting a few minutes for capacitors within the set to discharge or by turning off the set, removing the horizontal oscillator board (immediately resetting the circuit) and re-inserting it.

New crowbar description and schematic on page 5-30A. The anode over-voltage shutdown circuit consists of IC 1, SCR-1, and associated components. IC 1 is a voltage regulator (LM723LN) as used on the 15 and 30 volt regulator board 100, here employed in a different configuration to detect an over-voltage condition and trigger SCR-1. Refer to schematic on page 5-3A for IC 1 schematic. The temperature compensated reference voltage at pin 6 is divided by 5% resistors R20 and R22, adjusted by means of R-21, and applied to the inverting op-amp input at pin 4. The voltage at the non-inverting input pin 5, is proportional to anode voltage. Excessive high voltage will drive the op-amp output at pin 13 high and produce a high output at pin 9, triggering SCR-1 and turning on the LED. SCR-1 discharges C13 and thereby removes B+ from the horizontal oscillator. Note that B+ is generated from the 160 volt supply to insure quick starting of the oscillator. C12, C20, and C22 are integrating capacitors to insure that the circuit is not triggered by transients. 3 volt zener D7 protects the op-amp inputs. The oscillator, and therefore high voltage, will remain shut down until forward current to the SCR from the 160 V supply is removed, indicated by the LED turning off. This can be accomplished by momentarily removing, then re-inserting the horizontal oscillator board, or by turning the set off for a few minutes.

This horizontal oscillator board is interchangeable with other horizontal oscillator boards.

The horizontal oscillator also generates three waveforms that are synchronous with the scan current. The first is the horizontal ramp used in the phase detector circuitry, buffered to pin 7 by Q5. The other two are 30V pulses, one positive-going from ground (pin 4), and the other negative-going from +30V (Pin 1). These pulses are generated as the horizontal retrace pulse from pin 3 saturates Q7 (normally "off") and turns off Q8 (normally "on"). D9 and D10 prevent Q7 and Q8 from being driven too hard into saturation. Q9 and D11 provide a low impedance output to pin 4, while R47 limits current in the event of a short at pin 4.

(Q2 BASE WAVEFORM)

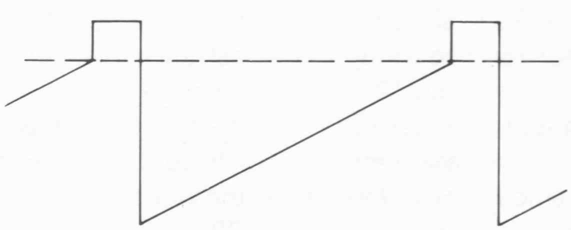


Figure Ia

WITHOUT RINGING CIRCUIT

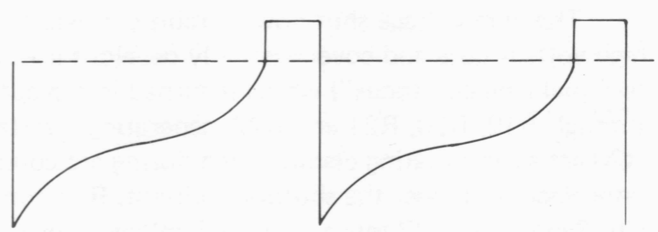


Figure Ib

WITH RINGING CIRCUIT

HIGH VOLTAGE CAGE AND COVER ASSEMBLY - A1800

The purpose of the high voltage cage and cover assembly is to generate horizontal scan current for the deflection yokes and also to generate anode voltage. The horizontal output (1800) circuit consists of a novel arrangement of silicon controlled rectifiers (SCR's) and diodes instead of the customary high voltage - high current transistor, while the high voltage section (including 1900) is of the flyback-driven voltage-multiplier type. Also included is a circuit which serves to regulate high voltage to 30kV $\pm$200V.

The horizontal output circuitry can best be explained with the simplified schematic shown in Figure A1800-1. The following table gives the correspondence between the components in the simplified schematic and the full schematic:

Fig I

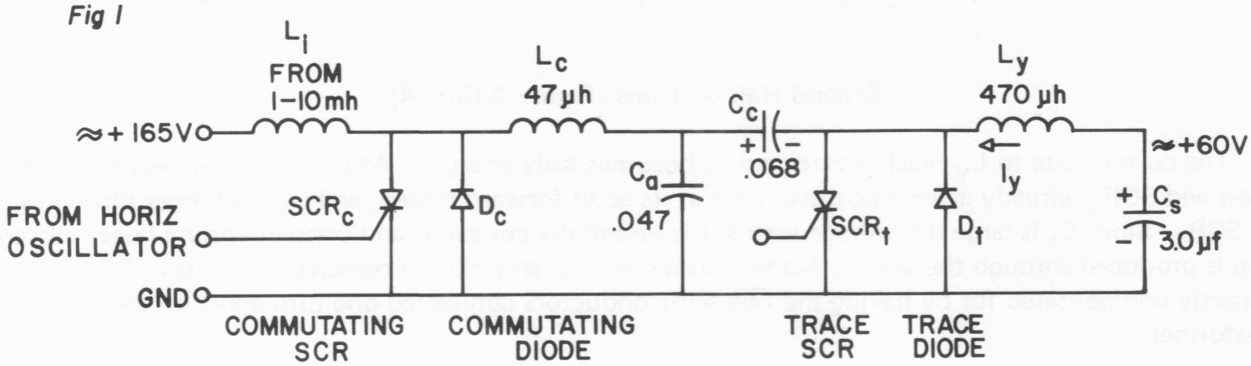


Figure A1800-1

Figure A1800-1 Designation	Schematic Designation	Description
C_s	C6, C7	"S Shaping" Capacitor
L_y		Width Coils, Horizontal Load Coil, Yokes (total inductance = 470 μH)
D_t	DA2	Trace Diode
SCR_t	SCR2	Trace SCR
C_c	CA3	Commutating Capacitor
L_c	LA1	Commutating Coil
D_c	DA1	Commutating Diode
SCR_c	SCR1	Commutating SCR
Ca	C3	Auxiliary Capacitor
Li	TA2, TA1	Parallel combination of TA2 (Input Inductor) and T1801 (Regulator Modulator)

The horizontal sweep (Figure A1800-2) can be broken down into five discrete intervals: first and second half of trace, during which the electron beam is swept across the raster; start of retrace, when a pulse from the horizontal oscillator prepares the circuit for retrace; and first and second half of retrace, during which the electron beam is quickly swept from right to left, in preparation for the new trace cycle. These five stages are marked by the successive opening and closing of the principal semiconductors, which may be thought of as switches. A diode conducts as long as there is a forward voltage drop and consequently, a forward current through it. It will "open up" should the current through it attempt to reverse. An SCR operates in much the same way, except that the point of forward current conduction (with a positive anode to cathode voltage) is a function of the gate voltage. The SCR remains in conduction until the current through it drops almost to zero.

First Half of Trace (Figure A1800-3)

Previous circuit action has developed a current in L_y of -4 amps (for a scan current of 8 A_{p-p}). Current flow is from the collapsing field in L_y through C_s and D_t. Note that even though the gate of SCR_t is given a positive pulse at this time, the voltage drop across D_t keeps it reverse-biased and thus non-conducting.

Second Half of Trace (Figure A1800-4)

The current due to L_y reaches zero and C_s becomes fully charged. At this point D_t becomes reverse-biased and SCR_t (already given a positive pulse at its gate) forward biased, and C_s discharges through L_y and SCR_t. Since C_s is large the voltage across it is essentially constant, and consequently a linear current ramp is produced through the yokes. Nonlinearities in this ramp due to resistive elements of SCR_t and D_t are partly compensated for by having the two semiconductors connected one turn apart on the high voltage transformer.

Start of Retrace (Figure A1800-5)

Shortly before time t_3 SCR_c receives a pulse from the horizontal oscillator and turns on. This action allows C_c, charged during trace time by L_i, to discharge into L_c and SCR_c, referred to as the commutating circuit. Due to the time constants involved this current increases rapidly in the form of a half-sine-wave pulse, and at time t_2 the retrace current exceeds the still-increasing trace current from C_s. As a result the net current through SCR_t becomes zero, and SCR_t turns off; the excess commutating current instead flows through D_t. However, as the retrace current falls, at time t_3 the excess commutating current is zero, and D_t opens up also. Now the current maintained by L_y flows entirely in the commutating circuit.

First Half of Retrace (Figure A1800-6)

With the trace switch open, the current from the series resonant commutating circuit flows through SCR_c and L_y, gradually falling to zero at time t_4 as C_c is charged to its peak negative value.

Second Half of Retrace (Figure A1800-7)

Current for the second half of retrace is derived from C_c's discharging from its peak negative value. This action returns the energy from the retrace capacitor back to the yoke inductance in preparation for the first half of the trace cycle. Current flow is through D_c, and the resultant forward voltage drop turns off SCR_c.

Just before time t_0, C_c has become discharged enough for D_t to become forward biased. As a result the commutating circuit is decoupled from the yokes and trace is initiated. The remaining commutating current decays rapidly to zero, and D_c opens up.

Energy is restored to the commutating circuit through the action of L_i (Figure A1800-8). During retrace L_i is connected between +160V and ground by SCR_c during the first half and by D_c during the second half. However, during trace time this path is broken, and consequently the energy from L_i charges C_c. Also, a winding on transformer TA2 (winding 3, 4 – see full schematic) develops a voltage during the charging of C_c which, after being shaped by C2, R3, R5, and L1, is used to forward bias SCR_t's gate for conduction during the second half of trace.

High voltage generation is accomplished by applying the retrace pulse (the voltage across the trace switch), to the primary of a step-up ("flyback") transformer, T 1901. The resultant pulses from the secondary are rectified and tripled to produce 30 kV. The anode current is returned to ground through J/P5 pin 8 at the RGB processor board (1300), where brightness limiting occurs. The Focus tap of the Tripler is used as a sense point for the over-voltage protection circuit on the horizontal oscillator board (1600). The resistors of the divider/bleeder function both as a high voltage discharge path for the three tubes when the set is turned off and also as a precise measure of the high voltage for the regulator circuitry.

Two circuits protect the Horizontal Output section in the event of high voltage arcing. The first consists of RA1 and CA4. These components act to damp any high-level ringing currents in the flyback transformer. The second circuit consists of D3, C4, C5, and R7. D3 charges C4 to the peak value of the retrace pulse; thus during arcing conditions the voltage on SCR_t can go no higher than this voltage. R7 provides a discharge path to the +160V supply.

High voltage regulation is accomplished by controlling the amount of energy that is supplied to the commutating capacitor during trace (Figure A1800-8). TA1 is a saturable reactor in parallel with TA2, the input inductor. In response to the regulator circuitry, Q1 pulls current from the +23V supply through TA1's control windings, thus varying TA1's inductance. This change in inductance modifies the resonance of TA2 (the 3, 4 winding) with CA3.

IC1 is an operational amplifier operated in both the inverting and also the non-inverting mode. In the non-inverting configuration, IC1 provides an error signal for Q1 by comparing a voltage reference at pin 4 with a sample of the high voltage at pin 5. R21, R22, and R23 provide a large range of high voltage adjustment by varying the value of the sense resistance in the high voltage divider. C14 sets the loop time constants for the regulator; the value is large so that the regulator will have essentially no effect during a field. If the regulator attempted to change the high voltage during a field, the change in scan current would show up on the screen as picture bending. Diodes D6 and D7 limit the range of differential input signals to 0.6V. The voltage reference for the inverting input is supplied by IC1 at pin 6, divided down by R16-R17 and filtered by R19-C13. The $\triangle$ H.V. control on the Kick Panel provides a small (±600V) range of high voltage adjustment by changing the reference voltage applied to pin 4. In the inverting configuration, the output of the amplifier at pin 9 is fed back to the input at pin 4 through R15. The closed-loop gain of the amplifier in this configuration is R15 divided by R18; the amplifier is compensated by C12.

The output of the chip is emitter-followed by both Q2 and Q1 to create a current in R11 and thus in the regulator modulator. RA2 serves to pull a constant 40 ma. through the control windings in order to allow the regulator modulator to operate in a linear region. During turn-on, base drive for transistor Q2 is provided by sampling the voltage across the "S shaping" capacitors, C6 and C7. Initially C8 is a "short" and the voltage across R10 forward biases D5. However, as C8 charges up D5 becomes reverse biased and base drive is provided by IC1 through R14.

C10, R13, and Q3 act to prevent the output of IC1 from rising too rapidly. Normally C10 is charged by R13 such that it follows the voltage on R12. Thus, when pin 9 rises rapidly the voltage on Q3's base remains constant until C10 charges to the new value; in this case Q3 turns on and draws current away from Q2's base.

Fig 2

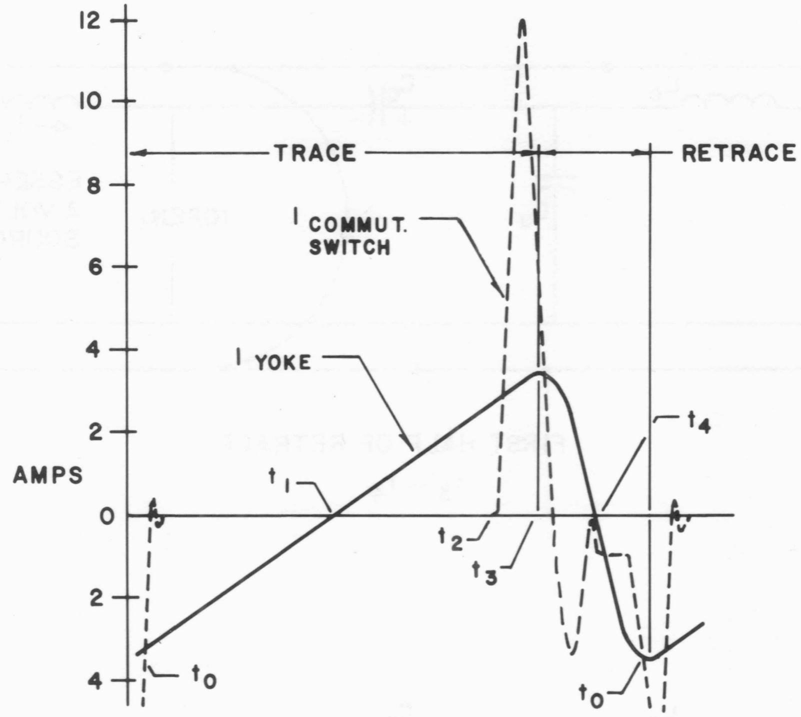
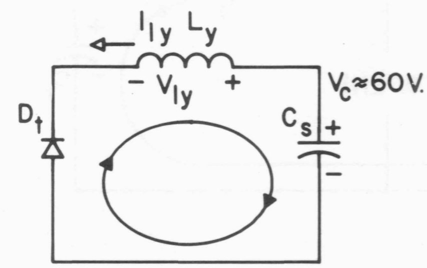
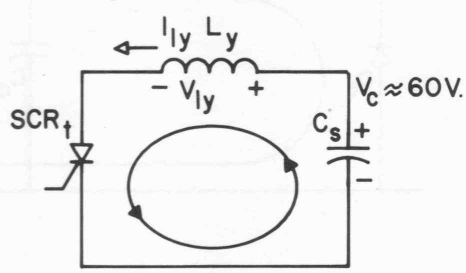


Fig 3



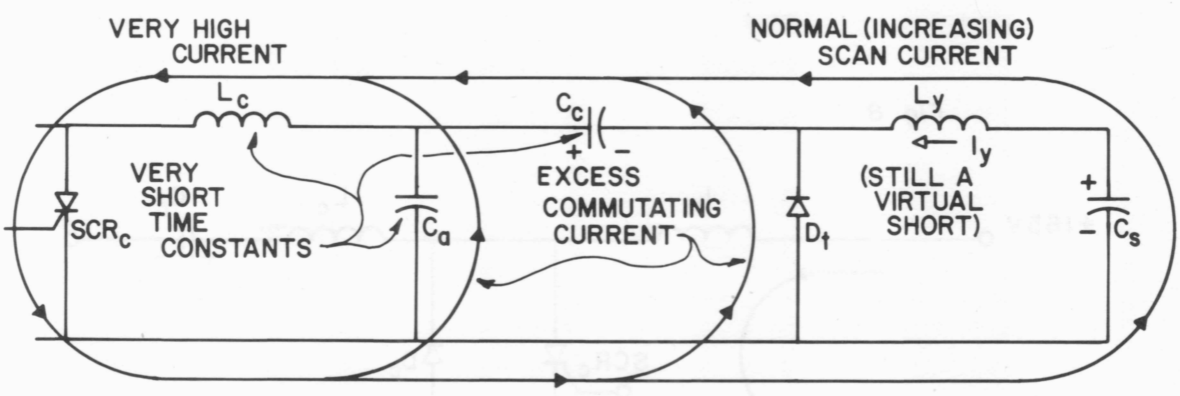
FIRST HALF
OF TRACE
$t_0 - t_1$

Fig 4



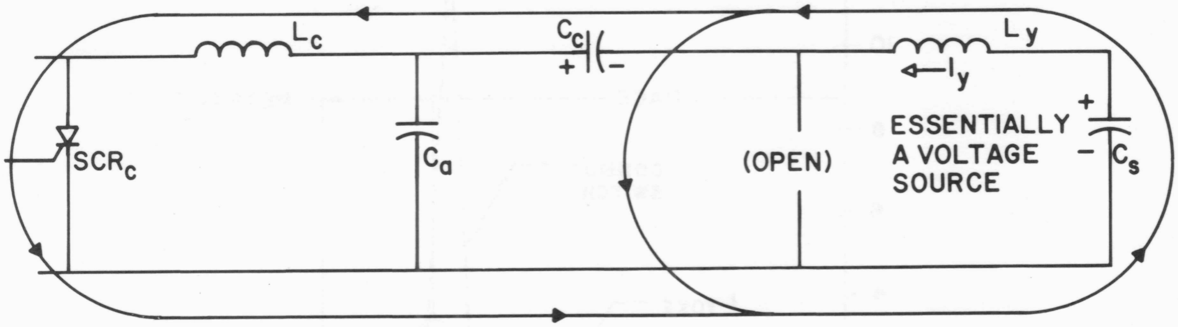
SECOND HALF
OF TRACE
$t_1 - t_2$

Fig 5



INITIATION OF RETRACE
$t_2 - t_3$

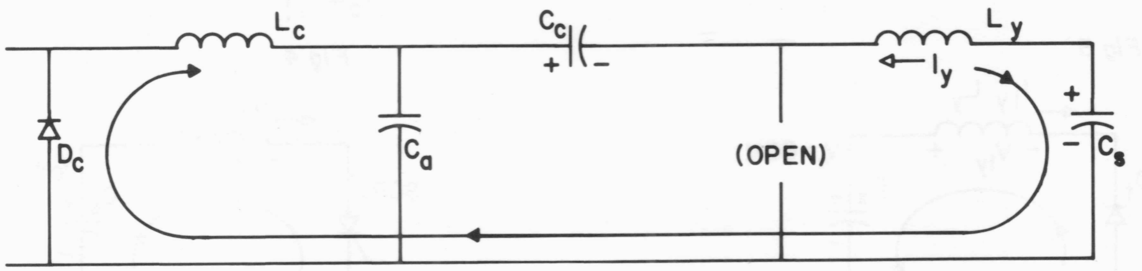
Fig 6



FIRST HALF OF RETRACE

$t_3 - t_4$

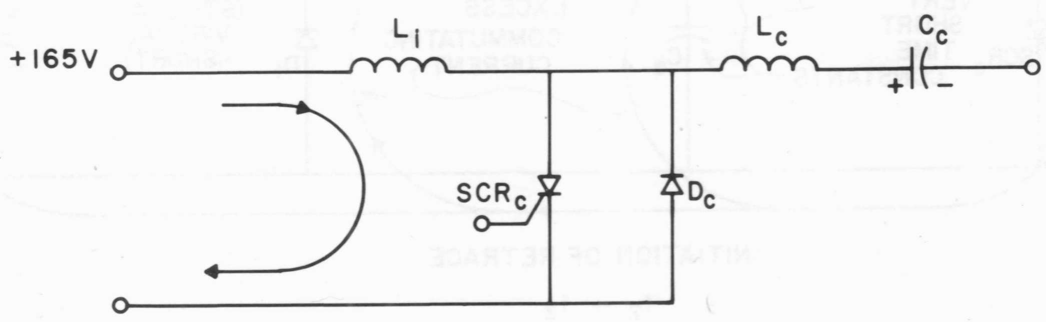
Fig 7



SECOND HALF OF RETRACE

$t_7 - t_0$

Fig 8



G2 DOUBLER AND REGULATOR – 2000

The G2 Doubler and Regulator generates a regulated 825 volt output which feeds the screen controls and thus the projection tube screen grids.

The 500 volt horizontal retrace pulse is applied to voltage doubler D1, C3, D2, C1, D3 and C2, generating a voltage of about 1000 volts. D1 conducts during retrace time, charging C3 to 500 volts. During trace time, D2 conducts, charging C1 from the voltage already on C3. The retrace pulse adds to the 500 volts on C1, and the sum is conducted by D3, placing 1000 volts on C2 and Q1.

The regulator consists of high-voltage transistor Q1 and small-signal devices Q2 and Q3. Q2 and Q3 form a differential pair, with current supplied by R5. Zener diode D4 supplies a reference voltage of about 30 volts, which is compared to Q2's base voltage, derived from R2, R3 and R4. Should the output voltage tend to go high, Q2's base becomes negatively biased with respect to Q3, channeling more current into R1, and reducing the output voltage. Closed loop compensation is provided by C5 and C4, with C4 also acting as a spark gap for protection against anode-to-screen arcs.

The output of the G2 Doubler and Regulator is connected through 10K isolation resistors to three dividers consisting of a SCREEN control and a 1M resistor. Inasmuch as the nominal output of the regulator is 825V, the SCREEN control determines a projection tube screen grid voltage between 412 and 825 volts. Further arc protection is supplied by 0.01 μf arc gap capacitors, 100K isolating resistors, and 0.75 pf 1KV arc gaps. Noise filtering is also accomplished by the 0.01 μf gap-caps. The controls for the red, green and blue tubes switch the second grid (screen) of that tube from the wiper of a screen control ("on") to a ground 470K resistor which slowly discharges the 0.01 μf capacitor and cuts off that projection tube ("off").

PINCUSHION CORRECTOR – 2100

The pincushion corrector modulates scanning currents from both the vertical and the horizontal deflection circuits in order to accomplish top and bottom and also side pincushion correction simultaneously. This is effected primarily through the action of T1, a saturable reactor.

Top and bottom pincushion correction requires that the amplitude of the vertical sweep current be modulated at a horizontal rate. Maximum correction occurs at the top and bottom of the picture, with zero correction at the center. This correction is generated through the resonance of C2 with T2 and the control windings of T1. This resonant current, modulated in saturable reactor T1, is added to the vertical scan current flowing to pin 7. T2 and R4 provide adjustment for the phase and the amplitude of the correction. Capacitor CA 115, mounted on the chassis near the vertical oscillator and amplifier board, bypasses the horizontal-rate modulation around the vertical amplifier.

Side pincushion correction requires that the horizontal sweep current be modulated at a vertical rate. The amplitude of the current for lines at the top and bottom of the screen must be decreased, while that for lines in the middle of the screen must be increased. This correction is effected by T1. The inductance of the load windings are varied at a vertical rate by vertical scan current flowing in the control windings. These load windings, tied to pins 1 and 2, are in parallel with the horizontal deflection yokes; thus the scan current is modulated at a vertical rate. No control over this correction is available.

Pins 5-6 and 11-12 provide an interlock function for the horizontal and vertical scanning circuit supply voltages to prevent damage to the cathode ray tubes and/or scan generators which would result from failure to install the pincushion generator.

7.5 VOLT REFERENCE BOARD – 2200

The 7.5 reference board is a stable, well-regulated voltage source, which can either source or sink current. It is used as a reference voltage for the DC-positioning controls, the DC positioning yokes, and the Keystone Amplifiers.

The circuit consists of differential pair Q1 and Q2, gain stage Q3, current source Q5, and output transistors Q4 and Q6 and has a closed-loop gain of 1. The voltage developed by divider R1 and R2 is compared to the output voltage and corrections are made by the amplifier such that the output voltage is equal to ½ the (+15V) input voltage. Thus the name, 7.5 Volt Reference.

C2 compensates the amplifier for its closed-loop gain of 1 and external capacitor (100 μf) keeps the dynamic impedance low.

FOCUS REGULATOR – 2300

The Focus Regulator delivers to the three projection tube focus coils a user-variable amount of incremental focus current for precise individual adjustment of focus.

The board consists of three individual circuits, one each for the blue, red and green focus coils. The front-panel FOCUS control applies a DC voltage between 0 and 4 volts to (for Blue) pin 5, where it is filtered by C1 and applied to the non-inverting input of a transconductance amplifier, which generates a proportional current between 0 and 200 ma. Differential-pair Q2 and Q4 are fed from current source Q3. Q5 supplies voltage amplification, and the closed-loop response is compensated by C3. Q6 provides current gain and drives the focus coil. Current flow is from the +23V supply through Q6, the focus coil and current sensing resistor R11, which is AC grounded by C4, R10 damps the inductive reactance of the coil for high frequency stability. The inverting input (Q4) is directly connected to R11, for 100% DC feedback. The current source is fed from R3, R6, and C2, which serve to decouple the ripple expected on the -9 volt supply, thus assuring low ripple modulation of the current source.

WAVEFORM GENERATOR — 2400

The Waveform Generator supplies the Dynamic Convergence Amplifiers with some of the signals necessary to correct for the different projection angles between each of the three projection tubes. Specifically, it generates a horizontal-rate ramp modulated by a vertical-rate ramp (known as the Keystone-Correction waveform), and amplifies positive and negative voltage replicas of the vertical scan current (±vertical ramp).

A sawtooth from the vertical deflection current sensing resistor (R1625) on the vertical amplifier board (1600) is low-pass-filtered by R16 and C5 to remove the horizontal-rate pincushion correction information. Q4 amplifies the ramp which C6 couples into the keystone generator and ramp amplifiers.

R26 supplies biasing current to zener diode D1, which maintains a reference voltage of 6.8 volts. This DC voltage is coupled to C6 by R25 and R24, setting the average value of the ramp applied to the keystone generator and insuring symmetry of the ramp about 6 volts. During horizontal retrace, a large positive pulse is coupled by R21 to Q5's gate, causing Q5 to become a low resistance, which effectively shorts C8 to C7 and D1. Thus C8 is clamped to 6 volts for about 12 microseconds at the horizontal rate. The voltage across R23 (a vertical ramp) causes a proportional amount of current to flow into C8 during trace time, thus generating a positive-or negative-going horizontal ramp. The large time constant of R23 and C8 insures linearity of the ramp, which is then buffered by Q6.

R24 and R25 also function as a voltage divider, feeding the vertical ramp signal to phase-inverter Q1. Q2 and Q3 provide low impedance outputs for the + and – ramps. C2 is a DC blocking capacitor whose large size is necessary to preserve low phase shift and ramp linearity at 60 Hz. R10, R12 and R14 are the three Horizontal Skew controls which provide for positive or negative correction for minor non-orthogonality in the main deflection yokes. The skew outputs are connected to the horizontal inverting (summing) inputs of the Dynamic Convergence Amplifiers through large value resistors on the chassis.

R8, R9 and C3 serve to subtract-out the vertical ramp component from the keystone signal, thus producing a symmetrical correction waveform. Q7 buffers this corrected keystone waveform and provides a low-impedance output, which is fed to the non-inverting inputs of the Dynamic Convergence Amplifiers.

BOW GENERATOR – 2500

The Bow Generator produces parabolic waveforms at both a horizontal and a vertical rate. These waveforms are used to correct for horizontal and vertical bow, and vertical nonlinearities in the raster (see Section 7).

In the vertical section, pin 10 receives a $3V_{p-p}$ negative-going ramp from the Vertical Oscillator and Amplifier (1600). This ramp, a voltage replica of the vertical scan current, is fed to Q1's base by R8 and C5. C6 removes horizontal pincushion information from the signal. The ramp is integrated by C2 to form a parabola. Q2 acts as a current source to supply the approximately 3 milliamperes required for Q1's DC biasing. The parabola at TP2 is then buffered to the various output pins by Q3 and Q4. R14 and R15 are necessary to keep the DC voltage at Q4's emitter below approximately 5V in order that C8, C9, and C10, which feed the summing inputs of the Blue and Green Dynamic Convergence Amplifiers (2600), are always properly biased. Q4 also acts as a phase splitter to provide inverted parabolas.

If the DC voltage on C2 is not to drift, then it is necessary that the current supplied by Q2 exactly equal that in Q1 as determined by the biasing resistors R2, R12, and R13. This balancing is accomplished by a feedback circuit which samples the DC voltage at Q1's collector and makes the necessary corrections to the voltage on Q2's base. For example, if Q2 is supplying too much current the voltage at TP2 will rise, and D1 will conduct, charging C7 (normally at 12V) to a higher voltage. This voltage results in a more positive voltage on Q2's base; consequently the current in Q2 decreases. R16 allows C7 to discharge enough during a field such that D1 conducts at the most positive points of each parabola.

The horizontal rate waveforms are generated in exactly the same manner, using a horizontal ramp from the Horizontal Oscillator (1700).

DYNAMIC CONVERGENCE AMPLIFIER – 2600

The Dynamic Convergence Amplifiers are dual linear transconducting/current amplifiers whose purpose is to drive the dynamic convergence yokes (one vertical and one horizontal yoke per tube for a total of 3 dual amplifiers per set).

The circuit is configured as a standard operational amplifier consisting of differential pairs Q1 and Q2, inverter Q3, current source Q4 and output transistors Q5 and Q6. The feedback goes to the base of Q2 where it is summed with the summing input but is not taken from the amplifier output but rather from return-current-sensing resistor R12. Yoke current flows from R8 or R9 through the dynamic convergence yokes and via pin 4 and R12 to the 7.5 volt reference source. Voltage is developed across R12 which is proportional to yoke current. R10 serves only to critically damp the yoke for the best retrace characteristics with minimum ringing. The closed-loop gain of the amplifier is determined by the amount of feedback which for DC is essentially 100% (the DC resistance of the yoke is less than 1 ohm).

The summing input is the inverting input while the non-inverting input is locally controlled by R1 and AC-coupled by C1 to the base of Q1. Q1 is biased by the 7.5 Ref. through R4 which for DC stability has the same values as R11.

For AC signals, the inductive component of the yoke impedance, while making the voltage waveform at the output terminal distorted, does not affect the non-reactive IR characteristics of sensing resistor R12. Consequently, an exact voltage replica of yoke current is developed across R12, which is fed back to Q2 by R11. Only high-value resistors are connected to the summing input, insuring negligible attenuation of the feedback signal, consequently Q2's base voltage closely follows the voltage on pin 4.

SCAN FAILURE PROTECTION – 2700

The purpose of the scan failure protection board is to positively blank off the projection tubes in the event of a failure in either deflection circuit. It also serves as an "instant off" device, blanking the screen upon shut-off.

Transistor Q5 is normally saturated, and the voltage at Pin 4 is about one volt less than at Pin 6. Pin 4 is connected to the tops of the G1 pots. The G1 pots have 110V across them inasmuch as the low sides of the pots are clamped to ground by a diode. Should a scan failure occur, then Q5 turns off and Pin 4 is allowed to float down to -160V, being pulled in that direction by an external resistor. It will remain at -160V, for there is no leakage path to ground to discharge the G1 and -160V supply capacitors from -160V even when the set is turned off.

The circuit consists of a dual two-stage amplifier, one for horizontal scan and one for vertical, an AND circuit (Q8 and Q3), a high voltage follower (Q4) and a high voltage switch (Q5). Pulses from an overwind on the Horizontal Load Coil are integrated by an external resistor and capacitor and applied to Pin 1. Transistors Q6 and Q7 are a two-stage amplifier with a gain determined by the ratio of R23 plus R19 over R20. This gain is adjusted such that the amount of sawtooth on Q7's collector is enough to trigger Q8. C11, D6, D7, and C12 form a voltage doubler. The negative side of C11 is clamped to a voltage no less than -0.6V on negative peaks of the sawtooth. On positive peaks, the negative end of C11 goes up to the peak to peak value of the signal, and the peak voltage is conducted through D7 to C12. C12 and R24 determine the time constant of the horizontal detector. D8 is a zener diode which sets a threshold voltage and as long as C12's voltage is larger than D8's firing voltage, then Q8 will saturate. The action of the top (vertical) amplifier is the same, although the component values are slightly different.

With Q8 and Q3 turned on, the voltage at Q3's collector will be 1 volt. Because Q4's base (and emitter) is held at +30V, 1ma flows through R12 and current-repeater transistor Q4. This constant current serves to saturate Q5.

Should the vertical scan fail, then Q3 would no longer get base current, and Q3's collector would go to +30V, turning off Q4 and Q5. Upon failure of Horizontal Scan, Q8 opens and the voltage on Q8's collector, base (D4 protects Q3 from zener breakdown) and emitter goes to +30V, shutting off Q4 and Q5.